THAT WHICH IS CLAIMED IS:

1. A quantum gate for carrying out a Grover's quantum algorithm using a certain binary function (f) defined on a space having a vector basis of n qubits, comprising

a superposition subsystem carrying out a superposition operation on components of input vectors for generating components (O11, O12; ...; O81, O82) of superposition vectors on a second vector basis of n+1 qubits,

an entanglement subsystem carrying out an entanglement operation on components of said linear superposition vectors for generating components (Q1, ..., Q8) of entanglement vectors, and

an interference subsystem carrying out an interference operation on components of said entanglement vectors for generating components of output vectors, comprising

at least an adder (HB25), input with signals representative of even or odd components of an entanglement vector (Q1, ..., Q8), generating a sum signal (SQ) representative of a weighted sum with a scale factor ($1/2^{n-1}$) of said even or odd components; an array of adders (HB16, ..., HB23), each input with a respective signal representing an even or odd component, respectively, of an entanglement vector (Q1, ..., Q8) and with said sum signal (SQ) and generating, as the difference between said sum signal (SQ) and a signal representing an even or odd component of an entanglement vector (Q1, ..., Q8), a signal representing, an even or odd component, respectively, of an output vector (A1, ..., A8).

2. The quantum gate of claim 1, comprising a processing subsystem having

at least an analog/digital converter (A/D), input with said signals representing even or odd components of an output vector (A1, ..., A8) for converting said signals in a digital string (DA1, ..., DA8);

a microprocessor unit (CPLD) input with said digital string (DA1, ..., DA8) for calculating a parameter to be made smaller than a certain threshold value (S) of said digital string of said converted components of the output vector (A1, ..., A8),

comparing said parameter (S) to be minimized with said threshold value for stopping the Grover's algorithm or commanding a further iteration thereof depending on whether said parameter (S) is smaller than said threshold value or not, respectively,

outputting a digital string (DIN) with said reduced parameter (S) representing components of said output vector;

at least a digital/analog converter (D/A) input with said digital string of reduced parameter (S) (DIN) for generating output signals (IN1, ..., IN8) corresponding to even or odd components of an output vector;

an array of inverters, each input with a respective output signal (IN1, ..., IN8) of said digital/analog converter D/A and generating a pair of signals of a certain voltage swing, representing opposite components (O11, O12; ...; O81, O82) of a new superposition vector that is input to said entanglement subsystem.

3. The quantum gate of claim 2, wherein

said analog/digital converter (A/D) is the commercial device ADC0808;

said microprocessor unit (CPLD) is the commercial device XC95288XL; and

said digital/analog converter (D/A) is the commercial device AD7228.

4. The quantum gate of claim 2, wherein said parameter (S) to be reduced is the Shannon entropy.

5. The quantum gate of claim 2, wherein said quantum gate has a modular architecture and comprises

an internal bus (BUS) for exchanging data among modules of said architecture and said microprocessor unit;

the microprocessor unit (CPLD) generating addresses (M) of the modules to be enabled to send to or receive data from said microprocessor on said bus, and logic signals first (OUT_EN) and second (WR) for enabling said analog/digital (A/D) and digital/analog converters (D/A), respectively;

one or more modules coupled to said internal bus (BUS), comprising

a respective subgroup of said array of inverters (INVERT) and of said array of adders (HB16, ..., HB23);

an identification circuit (SELECTOR) generating a relative bit string (R) that identifies a selected module;

a comparator input with the bit string (R) of the module and with said address (M), generating a flag

(ENABLE) that enables the module to exchange data with said microprocessor if the received address (M) matches with the bit string (R) of the module, otherwise sets the module in a tristate condition;

said analog/digital converter (A/D) being enabled by the logic AND between said flag (ENABLE) and said first logic signal (OUT_EN);

said digital/analog converter (D/A) being enabled by the logic AND between said flag (ENABLE) and said second logic signal (WR);

each of said adders (HB25) including a voltage buffer composed of an operational amplifier with an input connected by a resistor to a node at a respective input voltage (SQMX) of the buffer and at least a feedback resistor connected between an input and an output of the amplifier, outputting said sum signal (SQ), corresponding inputs and outputs of the operational amplifiers of the voltage buffers of the modules being connected in common.

6. The quantum gate of claim 5, wherein each voltage buffer comprises

a first voltage divider with a certain ratio composed of a pair of resistors, a first terminal node of which is coupled to a reference voltage and a second terminal node of which is coupled to the respective input voltage (SQMX) of the buffer;

a second voltage divider with the same ratio composed of another pair of resistors, a first terminal node of which is coupled to said reference voltage and a second terminal node of which is coupled to the output node of the operational amplifier;

said operational amplifier having a first input connected to the intermediate node of said first voltage divider and a second input connected to the intermediate node of said second voltage divider.

7. The quantum gate of claim 6, wherein each of said voltage dividers is composed of an identical pair of resistors.

8. The quantum gate of claim 5, wherein said input voltage (SQMX) of the buffer is a voltage representing a respective even or odd component of an entanglement vector (Q1, ..., Q8).

9. The quantum gate of claim 5, wherein said adder (HB25) of each module comprises also an auxiliary adder generating a respective partial sum signal representing a weighted sum of a respective pre-established number of even or odd components of said entanglement vector (Q1, ..., Q8) that is input to the respective buffer.

10. The quantum gate of claim 5, wherein said entanglement subsystem is constituted by

a command circuit (HB14) generating a number (2^n) of logic command signals (Vc1, ..., Vc8) encoding the values of said binary function (f) in correspondence of the vectors of the first basis;

an array of multiplexers (I-a), each driven by a respective logic command signal (Vc1, ..., Vc8) and input with a pair of signals (O11, O12; ...; O81, O82) representing components of a linear superposition vector that are referred to vectors of said second

basis having the first *n* qubits in common, and outputting, for each superposition vector (O11, ..., O82), corresponding signals representing components of an entanglement vector (Q1, ..., Q8), each component (Q1, ..., Q8) referring to a respective vector of the second basis being

equal to the corresponding component of the respective superposition vector, if said binary function (*f*) is null in correspondence of the vector of the first basis constituted by the first *n* qubits of said respective vector of the second basis, or

the opposite of the corresponding component of the respective superposition vector, if said binary function (*f*) is non null in correspondence of the vector of the first basis constituted by the first *n* qubits of said respective vector of the second basis;

each module comprising a respective subgroup (HB13) of said array of multiplexers (I-a) input with the components (O11, ..., O82) generated by said respective subgroup of said array of inverters (INVERT).

11. The quantum gate of claim 5, wherein said modules are identical to each other.

12. A method of carrying out an interference operation of a Grover's quantum algorithm, comprising the steps of

calculating a weighted sum (SQ) with a certain scale factor ($1/2^{n-1}$) of even or odd components of an entanglement vector (Q1, ..., Q8);

generating each even or odd component of an output vector by subtracting from said weighted sum

corresponding even or odd components, respectively, of an entanglement vector (Q1, ..., Q8).

13. The method of claim 12, comprising the steps of

calculating a number (2^{n-m}) of partial weighted sums (SQM1, SQM2), with a second scale factor ($1/2^{m-1}$), of a certain number (2^m) of even or odd components of an entanglement vector (Q1, ..., Q8);

calculating said weighted sum (SQ) by summing said partial weighted sums (SQM1, SQM2) with a second scale factor ($1/2^{n-m}$).